

WHAT IS CLAIMED IS:

- 1 1. A semiconductor memory device, comprising:
 - 2 a sense amplifier;
 - 3 first and second word lines;
 - 4 first and second bit lines coupled to said sense amplifier;
 - 5 a first memory cell coupled to said first word line and
 - 6 said first bit line; and
 - 7 a second memory cell coupled to said second word line and
 - 8 said second bit line;
 - 9 wherein, in a normal mode, the first and second word lines
 - 10 are assigned separate addresses from each other, and data access
 - 11 operation is performed in the first and second memory cells
 - 12 separately;
 - 13 whereas in a partial mode, the first and second word lines
 - 14 are assigned the same address to maintain one bit data in the
 - 15 first and second memory cells;
 - 16 wherein, in order to copy a data in the first memory cell
 - 17 into the second memory cell, based on a switching from the normal
 - 18 mode to the partial mode,
 - 19 the second word line is activated in a precharge period
 - 20 for the first and second bit lines, so that a precharge voltage
 - 21 is written into the second memory cell;
 - 22 then, the first word line is activated; and
 - 23 then, the sense amplifier is activated to amplify a
 - 24 differential voltage between the first and second bit lines to
 - 25 store said data stored in said first memory cell into said memory
 - 26 cell.

1 2. The device as claimed in claim 1, further comprising:
2 a trigger signal generator which generates a refresh
3 trigger signal to control a refresh operation of said first and
4 second memory cells, when the copying is entry, said trigger
5 signal generator generating said refresh trigger signal at a
6 first period which is the same as a period of said refresh trigger
7 signal generated at a period of said normal mode, then, said
8 trigger signal generator generating said refresh trigger signal
9 at a second period which is longer than said first period.

1 3. A semiconductor memory device, comprising:
2 a sense amplifier;
3 first and second word lines;
4 first and second bit lines coupled to said sense amplifier;
5 a first memory cell coupled to said first word line and
6 said first bit line; and
7 a second memory cell coupled to said second word line and
8 said second bit line;
9 wherein, in a normal mode, the first and second word lines
10 are assigned separate addresses from each other, and data access
11 operation is performed in the first and second memory cells
12 separately;
13 whereas in a partial mode, the first and second word lines
14 are assigned the same address to maintain one bit data in the
15 first and second memory cells; and
16 wherein, in order to copy a data in the first memory cell
17 into the second memory cell, based on a switching from the normal

18 mode to the partial mode,
19 the first word line is activated;
20 then, the sense amplifier is activated to amplify a
21 differential voltage between the first and second bit lines;
22 and
23 the second word line is activated, thereby storing said
24 data stored in said first memory cell into said memory cell;
25 when said copying is operated, said first word line is
26 activated at a first activate period, said second word line is
27 activated at a second active period which is shorter than said
28 first active period.

1 4. The device as claimed in claim 3, wherein
2 said first activate period is the same as that of said
3 first word line in said normal mode.

1 5. The device as claimed in claim 3, wherein
2 said second activate period is the same as that of said
3 first word line in said normal mode.

1 6. The device as claimed in claim 5, wherein
2 if a read/write access occurs at a time after the first
3 wordline is activated but before the second wordline is activated
4 during said partial mode, the first word line is activated for
5 the same period of time as the period of activating in the normal
6 mode and is thereafter inactivated, and activation of the second
7 word line is interrupted so that a read/write operation is
8 performed.

1 7. The device according to claim 6, wherein if a read/write
2 access occurs while the first word line is being activated and
3 after the second word line is activated during said partial mode,
4 the first word line is activated for a longer period than the
5 period of activating in the normal mode, the second word line
6 is activated for the same period as the activation period in
7 the normal mode, and then a read/write operation is performed.

1 8. The device according to claim 1, further comprising:
2 a timer to generate a trigger signal;
3 a delay circuit for delaying the trigger signal;
4 a first pulse-generating circuit for generating a first
5 one-shot pulse based on the output of the delay circuit;
6 a first word driver which receives said first one-shot
7 pulse to drive said first word line; and
8 a second pulse-generating circuit for generating a second
9 one-shot pulse based on the trigger signal;
10 a selector circuit which receives said first and second
11 one-shot pulses to output a selected one-shot pulse; and
12 a second word driver which receives said selected one-shot
13 pulse to drive the second word line.

1 9. The device according to claim 8, wherein:
2 said timer generates said trigger signal with a first cycle
3 and a second cycle which is different from said first cycle

1 10. The device according to claim 9, wherein:

2 said timer generates said trigger signal with said first
3 cycle when said copy is performed and generates said trigger
4 signal with said second cycle after said trigger signal with
5 said first cycle is generated.

1 11. The device according to claim 10, wherein
2 said first cycle is the same period as a cycle with when
3 said timer generates said trigger signal in said normal mode,
4 said second cycle has a period which is longer than that of said
5 first cycle.

1 12. The device according to claim 10, wherein
2 said first cycle has a period which is shorter than
3 that of a cycle with when said timer generates said trigger signal
4 in said normal mode, said second cycle has a period which is
5 longer than that of said cycle with when said timer generates
6 said trigger signal in said normal mode.

1 13. The device according to claim 3, further comprising:
2 a refresh timer which generates a trigger signal;
3 a frequency dividing circuit for dividing frequency of
4 the trigger signal;
5 a logic gate for performing a logical operation between
6 a chip select signal and a control signal for controlling the
7 normal mode and the partial mode;
8 a refresh cycle period-determining circuit for, based on
9 an output signal from the logic gate, determining a cycle period
10 of the trigger signal to be said first cycle period and then

11 to be a second cycle period longer than that of said first cycle
12 when the control signal indicates the partial mode and the chip
13 select signal is in an inactivated state, and determining the
14 cycle period of the trigger signal to be said first cycle period
15 when the chip select signal is in an activated state; and
16 a selector circuit for selecting an output signal from
17 the refresh timer when said determining circuit produces said
18 trigger signal with said first cycle and selecting a frequency
19 division signal from the frequency dividing circuit when said
20 determining circuit produces said trigger signal with said second
21 cycle.

1 14. The semiconductor memory device according to claim 13,
2 further comprising:
3 a circuit for generating a control signal for controlling
4 precharge of the bit lines and activation of the sense amplifier
5 based on the trigger signal output from the selector circuit,
6 an output signal from the refresh cycle period-determining
7 circuit, and an output signal from the logic gate;
8 a pulse generator for generating one-shot pulse, being
9 a core activating pulse, for controlling activation of the cell
10 array based on the trigger signal or detection of change of an
11 address supplied from outside of the semiconductor memory device;
12 a first logic gate for supplying an output of a first
13 predetermined result of a logical operation between the core
14 activating pulse and the control signal that controls the
15 precharge and the activation of the sense amplifier to a circuit
16 for precharging the bit lines; and

17 a second logic gate for supplying, as a sense
18 amplifier-activating signal, an output of a second predetermined
19 result of the logical operation between the core activating pulse
20 and the signal that controls the precharge and the activation
21 of the sense amplifier to the sense amplifier.

1 15. The semiconductor memory device according to claim 13,
2 further comprising:

3 a refresh address generator for generating a refresh
4 address signal based on the trigger signal output from the
5 selector circuit;

6 a first control circuit for generating a predetermined
7 bit signal and an inverted signal of the predetermined bit signal
8 based on a predetermined bit signal of the refresh address signal
9 that is output from the refresh address generator, an output
10 signal from the refresh cycle period-determining circuit, and
11 output signals from the logic gates; and

12 a second control circuit for controlling activation of
13 the first and second word lines based on, at least, the
14 predetermined bit signal, the inverted signal of the
15 predetermined bit signal, and an address signal corresponding
16 to the first word line.

1 16. A semiconductor memory device, comprising:

2 a sense amplifier;

3 first and second bit lines commonly coupled to said sense
4 amplifier;

5 first and second memory cells coupled to said first and

6 second bit lines; and respectively, said first and second memory
7 cells that stores and holds one bit data complementarily; wherein
8 when copying a data stored in one of the first and second
9 memory cells into the other one of the memory cells,
10 a data in the other one of the memory cells is reset;
11 after the resetting, a word line connected to the one of
12 the memory cells is activated;
13 after the activation, the data on the bit line read out
14 from the one of the cells is amplified by said sense amplifier
15 on said first and second bit lines; and
16 after amplified, the data is stored in the other memory
17 cell.

1 17. The device according to claim 16, wherein said reset is
2 performed by an operation such that a word line connected to
3 the other one of the memory cells in a precharge period for bit
4 lines.

1 18. A method of controlling a semiconductor memory device that
2 stores and holds one bit of data complementarily by two memory
3 cells respectively connected to two bit lines, which form a bit
4 line pair, commonly connected to one sense amplifier, the method
5 comprising the steps of:
6 resetting, when copying a cell data of one of the two memory
7 cells into the other one of the memory cells, a cell data of
8 the other one of the memory cells that is a copy destination;
9 and
10 activating, after resetting the other one of the memory

11 cells, a word line connected to the one of the memory cells,
12 amplifying by the sense amplifier the data of the one of the
13 memory cells to be output to the bit line pair, and storing the
14 cell data of the one of the memory cells into the other one of
15 the memory cells from the sense amplifier via the bit line pair.

1 19. The method of controlling a semiconductor memory device
2 according to claim 18, wherein the step of resetting the cell
3 data of the other one of the memory cells comprises a step of
4 writing an intermediate voltage into the other one of the memory
5 cells by activating a word line connected to the other one of
6 the memory cells in a period in which the bit line pair is
7 precharged to a precharge voltage being an intermediate voltage
8 between a high-potential side power supply voltage and a
9 low-potential side power supply voltage.

1 20. The method of controlling a semiconductor memory device
2 according to claim 19, wherein:
3 the two memory cells are respectively connected to two
4 word lines;
5 in a normal mode, the two word lines are assigned separate
6 addresses; and
7 in a twin cell mode in which one bit of data is
8 complementarily stored and held by the two memory cells, the
9 two word lines are assigned the same address and are activated
10 with the same timing after a cell data of one of the two memory
11 cells has been copied into the other one of the memory cells.

1 21. The method of controlling a semiconductor memory device
2 according to claim 20, wherein the copy operation of a data of
3 one of the two memory cells into the other one of the memory
4 cells is performed based on a trigger signal for instructing
5 a refresh operation of dynamic type memory cells.